CPRE 4910 Weekly Report 07

11/3/2025 - 11/10/2025

Group number: SDMay26-24

Project title: Digital ASIC Fabrication

Client &/Advisor: Dr. Henry Duwe

Team Members/Role:

Colin McGann	***-Project Lead***
Samuel Forde	***-PCB & Layout Lead***
Michael Drobot	***-Firmware Lead***
Jack Tonn	***-Testbench and Validation Lead***
Dawud Benedict	***-Toolflow Lead***
Emil Kosic	***-Repository and Coding Standards Lead***
Joshua Arceo	***-Client/Advisor Communications Lead***

- **Weekly Summary**

This week we continued work with the FPGA to get a basic image from the rasterizer. We made progress with the ISA and core design to prepare to start working on core Verilog. We also made progress in our build system for our custom software.

- **Past Week Accomplishments**
    - Colin McGann: Continued work on the FPGA integration of the rasterizer. Relized that the single cycle divider will not work on the FPGA. Got a pipelined divider written and will be integrating next week.
    - Jack Tonn: Further fleshed out core design and predication methods. Researched and developed the ISA for the cores.
    - Dawud Benedict: Started on the cache system and decided on a final memory hierarchy. Working on the PKBus-Wishbone interconnect.
    - Michael Drobot: Added more 3D models to our test dataset. Created datasheet LaTeX formatting macros to autogenerate register headers, register summary, and register descriptions. Integrated CustomASM into our build system and modified linker script to build assembled CustomASM programs into the final ELF file that's run on the management core. Created instructions and assembly syntax in CustomASM.

Created vertex shader and fragment shader test programs, and fixed ISA issues along the way.

- Sam Forde: Worked on learning SVUnit. Working on getting test mac units through synthesis.
- Josh Arceo: Created script to find reuse patterns of vertices within our object files, started writing a direct mapped, write through cache
- Emil Kosic: Continued test bench and synthesis of Register File. Continue core architecture research.

- **Pending Issues**
  - Get the SPI memory controller, PKBus, and VGA to work on the FPGA. The issues we found so far have been in the memory controller, in the PKBus stream protocol, the ChipForge FPGA tooling, and in Vivado's FPGA synthesis.
  - Research if the ISA is complete for the users, but not to feature creepy
  - Reexamine caching structure, potentially cache pre-shaded vertices.
- **Individual contributions**

NAME	Individual Contributions	Hours this week	HOURS cumulative
Colin McGann	FPGA and SPI memory controller work	10	110
Jack Tonn	Core model and ISA operations	10	51
Dawud Benedict	WB-PK bridge, Cadence tools	10	48
Michael Drobot	Datasheet LaTeX, CustomASM work	30	95
Sam Forde	Synthesizing mac unit	6	46
Josh Arceo	Reuse pattern scripts, start on cache	4	32
Emil Kosic	Core global and local registers	5	37

- **Plans for the upcoming week**
  - Colin McGann: Will continue working on our FPGA design and integrating the pipelined divider.
  - Jack Tonn: ALU verilog, ISA discussion and implementation
  - Dawud Benedict: Working on the Verilog for the cache systems.
  - Michael Drobot: Keep working on the ISA and shader programs, modifying the ISA as needed. Keep working on the core controller.

    - Sam Forde: Put together some performance analyses once mac test units have synthesized and area values are apparent.
    - Josh Arceo: Continue working on cache implementation, analyze script data to best implement our cache
    - Emil Kosic: Continue architecture research, design individual components

- **<u>Advisor Meeting Summary</u>**